TS5QSU21640-6S

品 名: __創見 2GB DDR2 667 SO-DIMM

創 見 料 號: TS5QSU21640-6S __

規 格: 2GB 200Pin SO-DIMM DDR2-667 Unbuffer Non-ECC Memory

廠 商: __研華科技股份有限公司__

廠 商 料 號: _____

日 期: _____

頁 數: _____

結 論: _____

Transcend *創見資訊股份有限公司*

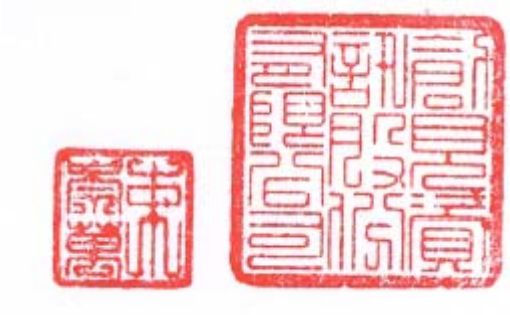
Your Supplier, Your Partner, Your Friend.

Transcend Information Inc.

地址：台北市內湖區行忠路 70 號

TEL： (886) 2-2792-8000

FAX： (886) 2-2793-2222/2-2796-8014



TS5QSU21640-6S

200PIN DDR2 667 SO-DIMM
2048MB With 128Mx8 CL5

Description

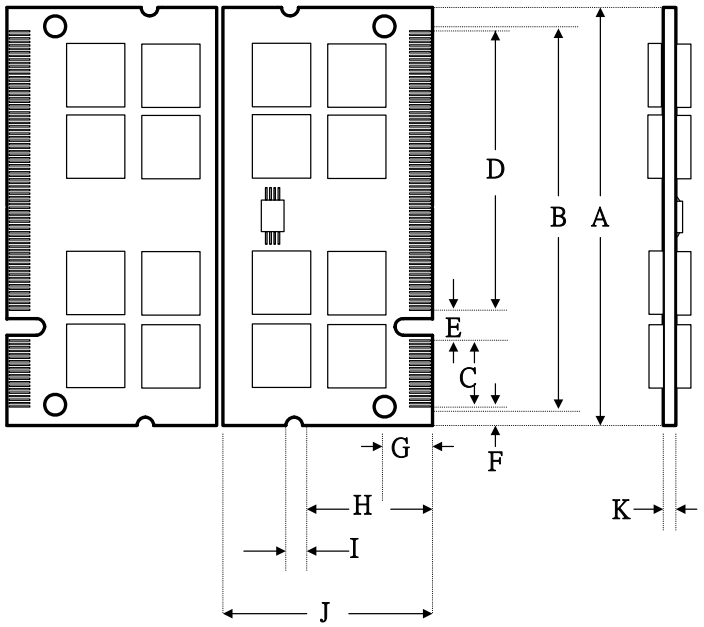
The TS5QSU21640-6S is a 256M x 64bits DDR2-667 SO-DIMM. The TS5QSU21640-6S consists of 16pcs 128Mx8bits DDR2 SDRAMs in 60 ball FBGA packages and a 2048 bits serial EEPROM on a 200-pin printed circuit board. The TS5QSU21640-6S is a Dual In-Line Memory Module and is intended for mounting into 200-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.8V ± 0.1V Power supply
- VDDQ=1.8V ± 0.1V
- Max clock Freq: 333MHZ; 667Mb/s/Pin.
- Posted CAS
- Programmable CAS Latency: 3,4,5
- Programmable Additive Latency :0, 1,2,3 and 4
- Write Latency (WL) = Read Latency (RL)-1
- Burst Length: 4,8(Interleave/nibble sequential)
- Programmable sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- MRS cycle with address key programs.
- On Die Termination
- Serial presence detect with EEPROM

Placement



PCB: 09-2164

Dimensions

Side	Millimeters	Inches
A	67.6±0.15	2.661±0.006
B	63.6	2.503
C	11.4	0.449
D	47.4	1.866
E	4.2	0.165
F	2.15±0.15	0.085±0.006
G	6	0.236
H	18	0.709
I	4	0.157
J	30	1.181
K	1.0±0.075	0.039±0.003

(Refer Placement)

Pin Identification

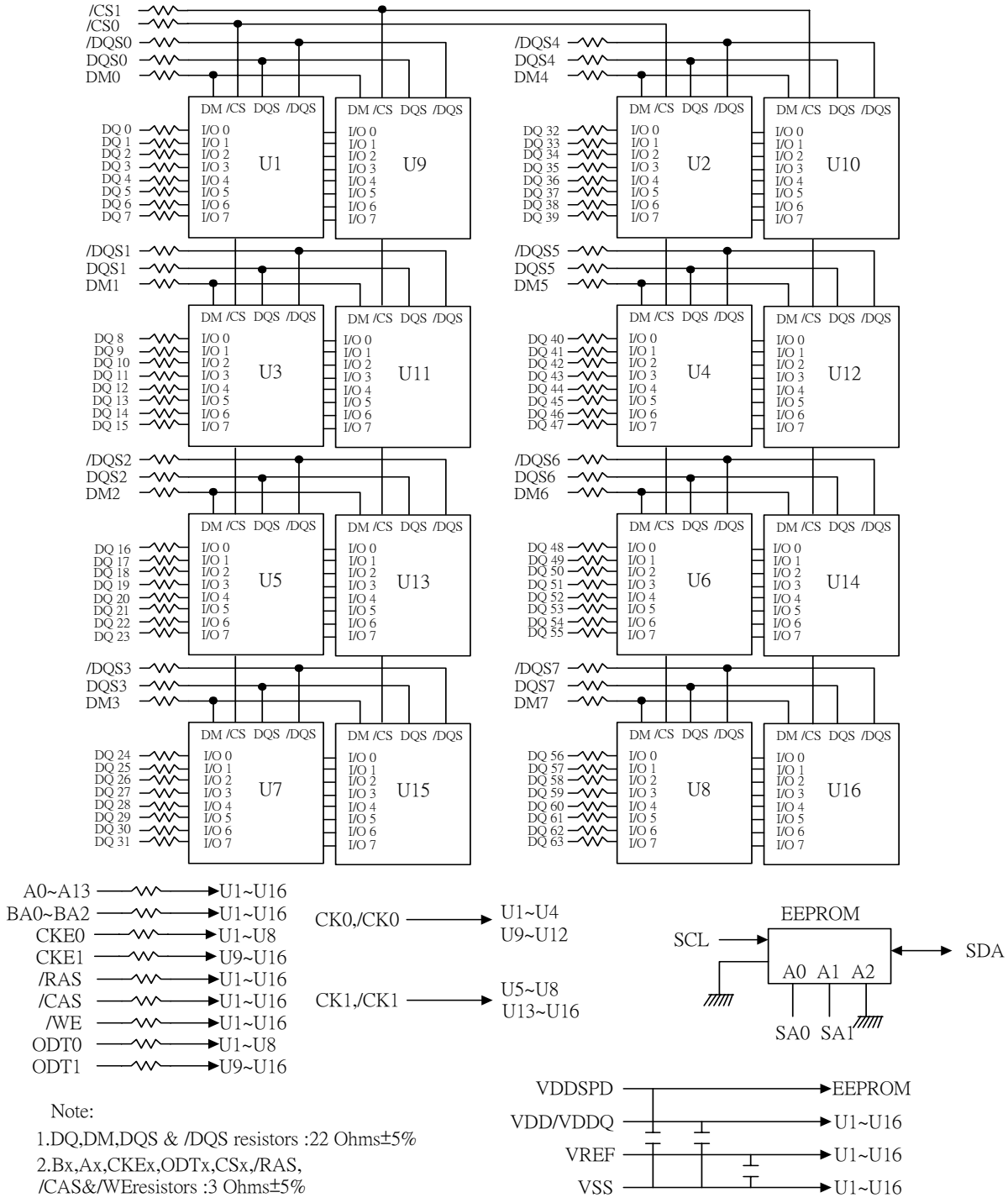
Symbol	Function
A0~A13, BA0~BA2	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobe
/DQS0~/DQS7	Differential Data strobe
CK0, /CK0 CK1, /CK1	Clock Input.
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data-in Mask
VDD	+1.8 Voltage power supply
VDDQ	+1.8 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	Serial EEPROM Positive Power Supply
SA0~SA2	Address select for EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	69	NC	137	DQ35	02	VSS	70	DQS3	138	VSS
03	VSS	71	VSS	139	VSS	04	DQ4	72	VSS	140	DQ44
05	DQ0	73	DQ26	141	DQ40	06	DQ5	74	DQ30	142	DQ45
07	DQ1	75	DQ27	143	DQ41	08	VSS	76	DQ31	144	VSS
09	VSS	77	VSS	145	VSS	10	DM0	78	VSS	146	/DQS5
11	/DQS0	79	CKE0	147	DM5	12	VSS	80	*CKE1	148	DQS5
13	DQS0	81	VDD	149	VSS	14	DQ6	82	VDD	150	VSS
15	VSS	83	*/CS2	151	DQ42	16	DQ7	84	*A15	152	DQ46
17	DQ2	85	*BA2	153	DQ43	18	VSS	86	*A14	154	DQ47
19	DQ3	87	VDD	155	VSS	20	DQ12	88	VDD	156	VSS
21	VSS	89	A12	157	DQ48	22	DQ13	90	A11	158	DQ52
23	DQ8	91	A9	159	DQ49	24	VSS	92	A7	160	DQ53
25	DQ9	93	A8	161	VSS	26	DM1	94	A6	162	VSS
27	VSS	95	VDD	163	NC, TEST	28	VSS	96	VDD	164	CK1
29	/DQS1	97	A5	165	VSS	30	CK0	98	A4	166	/CK1
31	DQS1	99	A3	167	/DQS6	32	/CK0	100	A2	168	VSS
33	VSS	101	A1	169	DQS6	34	VSS	102	A0	170	DM6
35	DQ10	103	VDD	171	VSS	36	DQ14	104	VDD	172	VSS
37	DQ11	105	A10/AP	173	DQ50	38	DQ15	106	BA1	174	DQ54
39	VSS	107	BA0	175	DQ51	40	VSS	108	/RAS	176	DQ55
41	VSS	109	/WE	177	VSS	42	VSS	110	/CS0	178	VSS
43	DQ16	111	VDD	179	DQ56	44	DQ20	112	VDD	180	DQ60
45	DQ17	113	/CAS	181	DQ57	46	DQ21	114	ODT0	182	DQ61
47	VSS	115	*/CS1	183	VSS	48	VSS	116	*A13	184	VSS
49	/DQS2	117	VDD	185	DM7	50	NC	118	VDD	186	/DQS7
51	DQS2	119	*ODT1	187	VSS	52	DM2	120	*/CS3	188	DQS7
53	VSS	121	VSS	189	DQ58	54	VSS	122	VSS	190	VSS
55	DQ18	123	DQ32	191	DQ59	56	DQ22	124	DQ36	192	DQ62
57	DQ19	125	DQ33	193	VSS	58	DQ23	126	DQ37	194	DQ63
59	VSS	127	VSS	195	SDA	60	VSS	128	VSS	196	VSS
61	DQ24	129	/DQS4	197	SCL	62	DQ28	130	DM4	198	SA0
63	DQ25	131	DQS4	199	VDDSPD	64	DQ29	132	VSS	200	SA1
65	VSS	133	VSS			66	VSS	134	DQ38		
67	DM3	135	DQ34			68	/DQS3	136	DQ39		

* Please refer Block Diagram

Block Diagram



Note:

1.DQ,DM,DQS & /DQS resistors :22 Ohms±5%

2.Bx,Ax,CKEx,ODTx,CSx,/RAS, /CAS&/WEresistors :3 Ohms±5%

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on V_{DD} relative to Vss	VDD	-1.0 ~ 2.3	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.5 ~ 2.3	V	1
Voltage on V_{DDL} pin relative to Vss	VDDL	-0.5 ~ 2.3	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 2.3	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.8)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.7	1.8	1.9	V	
Supply voltage for DLL	VDDL	1.7	1.8	1.9	V	4
Supply voltage for Output	VDDQ	1.7	1.8	1.9	V	4
I/O Reference voltage	VREF	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	1,2
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
DC Input logic high	$V_{IH(DC)}$	V_{REF}+0.125	-	V_{DDQ}+0.3	V	
DC Input logic low	$V_{IL(DC)}$	-0.3	-	V_{REF}-0.125	V	

Note:
There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed +/-2% VREF (DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

IDD Specification parameters Definition

(IDD values are for full operating range of voltage and Temperature)

Parameter		Symbol	Max.	Unit	Note
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0	1,120	mA	
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD1	1,520	mA	
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P	112	mA	
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q	640	mA	
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD2N	640	mA	
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	IDD3P-F	480	mA	
	Slow PDN Exit MRS(12) = 1mA	IDD3P-S	160		
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD3N	720	mA	
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD4R	2,000	mA	
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R		IDD4W	2,000	mA	
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD5	3,360	mA	
Self refresh current; CK and CK\ at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		IDD6	112	mA	
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		IDD7	4,320	mA	

Note: 1. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading capacitor.

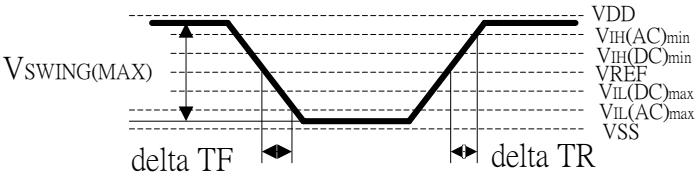
Input AC Logic Level

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.200		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.200	V	

AC Input Test Condition

Condition	Symbol	Value	Unit	Note
Input reference voltage	VREF	0.5*VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(MAX)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/ns	2,3

Note: 1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.



$$\text{Falling Slew} = \frac{V_{REF} - V_{IL}(AC)_{max}}{\text{delta TF}} \qquad \text{Rising Slew} = \frac{V_{IH}(AC)_{min} - V_{REF}}{\text{delta TR}}$$

AC Input Test Signal Waveform

Input/Output Capacitance (V_{DD} = 1.8V, V_{DDQ} = 1.8V, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK0 and /CK0)	CCK0	-	48	pF
Input capacitance (CK1 and /CK1)	CCK1	-	48	pF
Input capacitance (CKE and /CS)	CI1	-	42	pF
Input capacitance (A0~A13, BA0~BA2, /RAS, /CAS, /WE)	CI2	-	42	pF
Input capacitance (DQ, DM, DQS, /DQS)	CIO	-	9	pF

Note: DM is internally loaded to match DQ and DQS identically.

Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
DQ output access time from CK & /CK	tAC	-450	+450	ps	
DQS output access time from CK & /CK	tDQSCK	-400	+400	ps	
CK high-level width	tCH	0.48	0.52	tCK	
CK low-level width	tCL	0.48	0.52	tCK	
CK half period	tHP	min(tCL,tCH)	X	ps	
Clock cycle time, CL=x	tCK	3000	8000	ps	
DQ and DM input hold time	tDH	175	x	ps	
DQ and DM input setup time	tDS	100	X	ps	
Control & Address input pulse width for each input	tIPW	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	X	tCK	
Data-out high-impedance time from CK/CK	tHZ	X	tAC max	ps	
DQS low-impedance time from CK/CK	tLZ(DQS)	tAC min	tAC max	ps	
DQ low-impedance time from CK/CK	tLZ(DQ)	2*tAC min	TAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	X	240	ps	
DQ hold skew factor	tQHS	X	340	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	X	ps	
Write command to first DQS latching transition	tDQSS	-0.25	+0.25	tCK	
DQS input high pulse width	tDQSH	0.35	X	tCK	
DQS input low pulse width	tDQSL	0.35	X	tCK	
DQS falling edge to CK setup time	tDSS	0.2	X	tCK	
DQS falling edge hold time from CK	tDSH	0.2	X	tCK	
Mode register set command cycle time	tMRD	2	X	tCK	
Write postamble	tWPST	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	X	tCK	
Address and control input hold time	tIH	275	X	ps	
Address and control input setup time	tIS	200	X	ps	
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Active to active command period for 1KB page size products	tRRD	7.5	X	ns	
Active to active command period for 2KB page size products	tRRD	10	X	ns	
Four Activate Window for 1KB page size products	tFAW	37.5		ns	
Four Activate Window for 2KB page size products	tFAW	50		ns	

/CAS to /CAS command delay	tCCD	2		tCK	
Write recovery time	tWR	15	X	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP	X	tCK	
Internal write to read command delay	tWTR	7.5	X	ns	
Internal read to precharge command delay	tRTP	7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		tCK	
Exit precharge power down to any non-read command	tXP	2	X	tCK	
Exit active power down to read command	tXARD	2	X	tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		tCK	
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		tCK	
ODT power down exit latency	tAXPD	8		tCK	
OCD drive mode output delay	tOIT	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		ns	

SERIAL PRESENCE DETECT SPECIFICATION

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Serial PD Bytes written during module production	128bytes	80
1	Total # of Bytes of S.P.D Memory Device	256bytes	08
2	Fundamental Memory Type	DDR2 SDRAM	08
3	# of Row Addresses on this Assembly	14	0E
4	# of Column Addresses on this Assembly	10	0A
5	# of Module Rows on this Assembly	2 ROW, Planar, 30.0mm	61
6	Data Width of this Assembly	64bits	40
7	Reserved	-	00
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V	05
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.00ns	30
10	DDR2 SDRAM Access time from clock at CL=X	±0.45ns	45
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC	00
12	Refresh Rate	7.8us	82
13	Primary DDR2 SDRAM Width	X8	08
14	Error Checking DDR2 SDRAM Width	N/A	00
15	Reserved	-	00
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8	0C
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	8 banks	08
18	DDR2 SDRAM device attributes:CAS Latency supported	5,4,3	38
19	DIMM Mechanical Characteristics	X=<3.80	01
20	DIMM type information	SODIMM	04
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable	00
22	DDR2 SDRAM Device Attributes: General	Supports weak driver	03
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns	3D
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns	50
25	DDR SDRAM Cycle Time CL=X-2	5.0ns	50
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns	60
27	Minimum Row Precharge Time (tRP)	15ns	3C
28	Minimum Row Active to Row Activate delay (tRRD)	7.5ns	1E
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C
30	Minimum active to Precharge time (tRAS)	45ns	2D
31	Module ROW density	1GB	01
32	Command and address setup time before clock(=tIS)	0.20ns	20
33	Command and address hold time after clock(=tIH)	0.27ns	27
34	Data input setup time before strobe(=tDS)	0.10ns	10
35	Data input hold time after strobe(=tDH)	0.17ns	17
36	Write recovery time(=tWR)	15ns	3C

37	Internal write to read command delay(=tWTR)	7.5ns	1E					
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E					
39	Memory analysis probe characteristics	-	00					
40	Reserved	-	06					
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	60ns	3C					
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	127ns	7F					
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns	80					
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.24ns	18					
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.34ns	22					
46	PLL Relock Time	-	00					
47~61	Superset Information	-	00					
62	SPD Data Revision Code	REV 1.2	12					
63	Checksum for Bytes 0-62	13	15					
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS5QSU21640-6S	54	53	32	35	36	4D
			53	51	36	34	56	36
			55	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Open for customer use	Undefined	-					