



SY88149HL

3.3V 1.25Gbps Burst-Mode Limiting Amplifier with Ultra-Fast Signal Assert Timing

General Description

The SY88149HL is a high-sensitivity, burst-mode capable limiting post amplifier designed for Optical Line Terminal (OLT) receiver applications. The SY88149HL satisfies the strict timing restrictions of the GPON standards by providing ultra-fast Loss-of-Signal (LOS) or Signal-Detect (SD) output. Auto Reset and Manual Reset options are provided to control LOS/SD output timing. For increased flexibility, this device also includes an option to select between LOS or SD output. The device can be connected to burst-mode capable transimpedance amplifiers (TIAs) using AC or DC coupling.

The SY88149HL generates a high-gain LOS or SD LVTTTL output. A programmable LOS/SD level pin (LOS/SD_{LVL}) sets the sensitivity of the input amplitude detection. This device also offers the option to choose between a Loss-of-Signal (LOS) and a Signal-Detect (SD) output from the LOS/SD pin based the LOS/SDSEL pin setting. To select SD output, leave LOS/SDSEL pin open or connect to V_{cc} ; to select LOS output, tie LOS/SDSEL-to-ground. If the input signal amplitude falls below the threshold set by LOS/SD_{LVL} , LOS will assert high (or SD will de-assert low). Once the input signal rises above the threshold set by LOS/SD_{LVL} , LOS will de-assert low (or SD output will assert high). The SY88149HL also features a JAM function which, when active, disables the LVPECL outputs. JAM is active LOW when SD is selected and active HIGH when LOS is selected. The LOS/SD output should be fed back to the JAM input to maintain output stability under an invalid signal condition. Typically, 3dB SD hysteresis is provided to prevent chattering.

The SY88149HL operates from a single +3.3V power supply over temperatures ranging from -40°C to $+85^{\circ}\text{C}$. With its wide bandwidth and high gain, signals up to 1.25Gbps and as small as 4mVpp can be amplified to drive devices with LVPECL inputs.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single 3.3V power supply
- <5ns SD assert (LOS de-assert) time
- Option to AUTORESET or Manual RESET LOS output to HIGH and SD output to LOW
- Option to select LOS or SD output
- Up to 1.25Gbps operation
- Low-noise differential LVPECL data outputs
- 4mVpp input sensitivity
- High sensitivity LOS/SD detect
- Ultra fast LVTTTL LOS/SD output
- Squelching function to disable output
- Programmable LOS/SD level set (LOS/SD_{LVL})
- Available in a 16-pin (3mmx 3mm) QFN package

Applications

- GE-PON/GPON/EPON OLT
- Gigabit Ethernet
- Fibre Channel
- OC-3/12/24 SONET/SDH
- High-gain line driver and line receiver
- Low-gain TIA interface

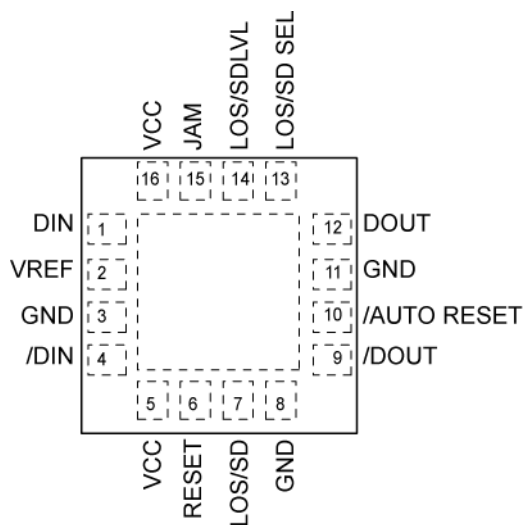
Markets

- FTTH/FTTP
- Datacom/Telecom
- Optical transceiver

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88149HLMG	QFN-16	Industrial	149H with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88149HLMGTR ⁽¹⁾	QFN-16	Industrial	149H with Pb-Free bar-line indicator	NiPdAu Pb-Free

Pin Configuration



16-Pin QFN

Truth Tables

LOS/SDSEL	Function	LOS/SD Output (JAM Input)	OUTPUTS
High	SD	High	Enabled
High	SD	Low	Disabled
Low	LOS	Low	Enabled
Low	LOS	High	Disabled

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	DIN, /DIN	Data Inputs. If AC-Coupled, terminate each pin to Vref with 50Ω.
2	VREF	Reference Voltage Output. Typically Vcc – 1.3V.
3,11,8	GND	Device Ground. Exposed pad must be soldered (or equivalent) to the same potential as ground pins.
10	/AUTORESET	LVTTTL Input. This pin is internally connected to a 25kΩ pull-up resistor and defaults to HIGH. When this pin is LOW or tied to ground, the /AUTORESET function is enabled and SD de-asserts or LOS asserts within 100ns (typical) after the last high to low transition of the burst input. When this pin is left floating or not connected, the AUTORESET function is disabled and the SD de-assert or LOS assert must be forced by using the manual RESET function.
5,16	VCC	Positive power supply. Bypass with 0.1uF 0.01uF low ESR capacitors. 0.01uF capacitors should be as close as possible to VCC pins.
6	RESET	LVTTTL Input. Apply a high-level signal (>2V) to this pin to discharge the time constant and reset the signal de-assert time or LOS assert time within 5ns. RESET defaults to Low if left floating. If the /AUTORESET function is not used, this RESET function needs to be used to quickly de-assert the SD or assert LOS. Note that this input is internally connected to a 25kΩ pull-up resistor.
7	LOS/SD	LVTTTL Output. Signal-Detect (SD) asserts high when the data input amplitude rises above the threshold set by SD _{LVL} . Conversely, Loss-of-Signal (LOS) de-asserts low when the data input amplitude rises above the threshold set by LOS _{LVL} .
12, 9	DOUT, /DOUT	LVPECL Outputs. When JAM disables the device, output DOUT is forced to logic LOW and output /DOUT is forced to logic HIGH.
13	LOS/SDSEL	LVTTTL Input. Connect to V _{CC} or leave open to select SD; set low or connect-to-GND to select LOS. This pin also controls the LOS/SD output and polarity of the JAM function. When SD is selected, JAM is active LOW and LOS/SD (pin 7) operates as signal detect. Conversely, when LOS is selected, JAM is active HIGH and LOS/SD operates as loss-of-signal. Note that this input is internally connected to a 25Ω pull-down resistor
14	LOS/SDLVL	Voltage Input. Sets the Loss of Signal/Signal Detect Level. A resistor from this pin to V _{CC} sets the threshold for the data input amplitude at which LOS/SD will be asserted.
15	JAM	LVTTTL Input. JAM acts as a squelch function which can disable the LVPECL outputs. The polarity of the input that triggers an active JAM depends upon LOS/SDSEL status. When LOS is selected, this pin is active HIGH. When SD is selected, this pin is active LOW. To create a squelch function, connect JAM to LOS/SD output. When JAM disables the device, output Q is forced to logic LOW and output /Q is forced to logic HIGH. Note that this input is internally connected to a 25kΩ pull-up resistor.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	0V to +4.0V
Input Voltage (DIN, /DIN)	0 to V_{CC}
Output Current (I_{OUT})	
Continuous	$\pm 50\text{mA}$
Surge	$\pm 100\text{mA}$
TTL Inputs Voltage	0 to V_{CC}
V_{REF} Current	-800 μA to +500 μA
LOS/SD _{LVL} Voltage	V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature (T_s)	-65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	+3.0V to +3.6V
Ambient Temperature (T_A)	-40°C to +85°C
Junction Temperature (T_J)	-40°C to +125°C
Junction Thermal Resistance ⁽³⁾	
QFN (θ_{JA}) Still-air	60°C/W
QFN (Ψ_{JB}) Junction-to-board	38°C/W

DC Electrical Characteristics

$V_{CC} = 3.0$ to 3.6V ; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, typical values at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		57	78	mA
LOS/SD _{LVL}	LOS/SD _{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	LVPECL Output HIGH Voltage	50 Ω to $V_{CC}-2\text{V}$	$V_{CC}-1.085$	$V_{CC}-0.955$	$V_{CC}-0.880$	V
V_{OL}	LVPECL Output LOW Voltage	50 Ω to $V_{CC}-2\text{V}$	$V_{CC}-1.830$	$V_{CC}-1.705$	$V_{CC}-1.555$	V
I_{OFFSET}	Input Offset Voltage				1	mV
V_{IHCMR}	Common Mode Range		GND+2.0		V_{CC}	V
V_{REF}	Reference Voltage		$V_{CC}-1.48$	$V_{CC}-1.32$	$V_{CC}-1.16$	V

LVTTL DC Electrical Characteristics

$V_{CC} = 3.0$ to 3.6V ; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, typical values at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	TTL Input HIGH Voltage		2.0			V
V_{IL}	TTL Input LOW Voltage				0.8	V
I_{IH}	TTL Input HIGH Current (/AUTORESET, JAM, LOS/SDSEL)	$V_{IN} = 2.7\text{V}$ $V_{IN} = V_{CC}$			20 100	μA μA
I_{IL}	TTL Input LOW Current (/AUTORESET, JAM, LOS/SDSEL)	$V_{IN} = 0.5\text{V}$	-0.3			mA
I_{IH}	TTL Input HIGH Current (RESET)	$V_{IN} = 2.7\text{V}$ $V_{IN} = V_{CC}$			200 300	μA μA
I_{IL}	TTL Input LOW Current (RESET)	$V_{IN} = 0.5\text{V}$	-0.05			mA
V_{OL}	TTL Output LOW Level	$I_{OL} = +20\text{mA}$			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

AC Electrical Characteristics

$V_{CC} = 3.0V$ to $3.6V$; $R_{LOAD} = 50\Omega$ to $V_{CC}-2V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4			260	ps
t_{JAM_LH}	JAM Low to High Propagation Time	Note 12			5	ns
t_{JAM_HL}	JAM High to Low Propagation Time	Note 13			2	ns
$t_{AUTORESET}$	SD de-assert or LOS assert with Auto Reset enabled.		75	100	150	ns
t_{RESET}	RESET time constant	Note 5			5	ns
t_{ON}	SD Assert Time/LOS De-assert time	Note 9			5	ns
t_{JITTER}	Deterministic Random	Note 6 Note 7		15 5		ps _{PP} ps _{RMS}
V_{ID}	Differential Input Voltage Swing	Figure 1	4		1800	mV _{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$		1500		mV _{PP}
SD_{AL}/LOS_{DL}	Low SD Assert/LOS De-assert Level	$R_{LOS/SDLVL} = 5k\Omega$, Note 8, 10		4.2		mV _{PP}
SD_{DL}/LOS_{AL}	Low SD De-assert/LOS Assert Level	$R_{LOS/SDLVL} = 5k\Omega$, Note 10		3		mV _{PP}
HYS_L	Low SD/LOS Hysteresis	$R_{LOS/SDLVL} = 5k\Omega$, Note 11		2.9		dB
SD_{AM}/LOS_{DM}	Medium SD Assert/LOS De-assert Level	$R_{LOS/SDLVL} = 2.5k\Omega$, Note 10		5.2	12	mV _{PP}
SD_{DM}/LOS_{AM}	Medium SD De-assert/LOS Assert Level	$R_{LOS/SDLVL} = 2.5k\Omega$, Note 10	2.5	3.7		mV _{PP}
HYS_M	Medium SD/LOS Hysteresis	$R_{LOS/SDLVL} = 2.5k\Omega$, Note 11		3		dB
SD_{AH}/LOS_{DH}	High SD Assert/LOS De-assert Level	$R_{LOS/SDLVL} = 50\Omega$, Note 10		15	24	mV _{PP}
SD_{DH}/LOS_{AH}	High SD De-assert/ LOS Assert Level	$R_{LOS/SDLVL} = 50\Omega$, Note 10	6	9.5		mV _{PP}
HYS_H	High SD/LOS Hysteresis	$R_{LOS/SDLVL} = 50\Omega$, Note 11		4		dB
B_{-3dB}	3dB Bandwidth			1		GHz
$A_{V(Diff)}$	Differential Voltage Gain			48		dB
S_{21}	Single-ended Small-Signal Gain			42		dB

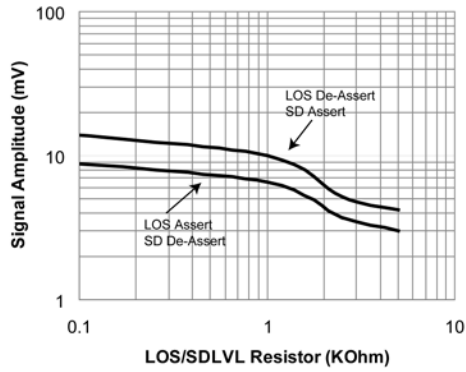
Notes:

- Amplifier in limiting mode. Input is a 200MHz square wave.
- The time between applying RESET and outputs being disabled.
- Deterministic jitter measured using 1.25Gbps K28.5 pattern, $V_{ID} = 10mV_{PP}$.
- Random jitter measured using 1.25Gbps K28.7 pattern, $V_{ID} = 10mV_{PP}$.
- SD is the opposite polarity of LOS. Therefore, an SD Assert parameter is equivalent to a LOS De-assert parameter and vice versa.
- See "Typical Operating Characteristics" for graphs showing input signal vs. SD Assert/LOS De-assert time at various $R_{LOS/SDLVL}$ settings.
- See "Typical Operating Characteristics" for a graph showing how to choose a particular $R_{LOS/SDLVL}$ for a particular assert and its associated de-assert amplitude.
- This specification defines electrical hysteresis as $20\log(SD \text{ Assert}/SD \text{ De-assert})$. The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-5dB, shown in the AC characteristics table, will be: 1dB-4dB optical Hysteresis.
- JAM Low to High transition propagation delay refers to the time it takes from a LOW to HIGH transition at JAM input to turning on (if SD is selected) or turning off (if LOS is selected) the LVPECL outputs.
- JAM High to Low transition propagation delay refers to the time it takes from a HIGH to LOW transition at JAM input to turning off (if SD is selected) or turning on (if LOS is selected) the LVPECL outputs.

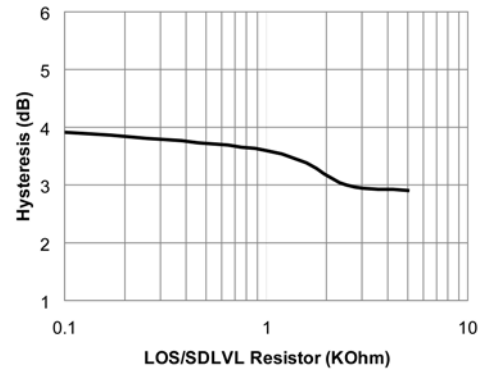
Typical Operating Characteristics

$V_{CC} = 3.3V$, $T_A = 25^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

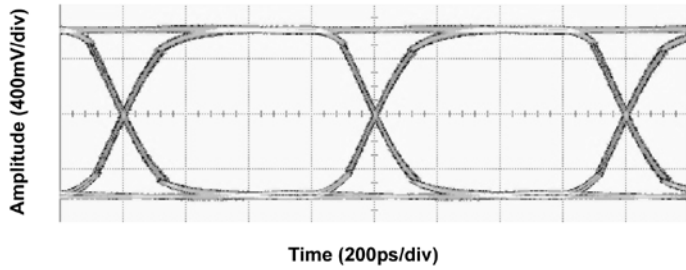
LOS & SD Assert/De-Assert Levels



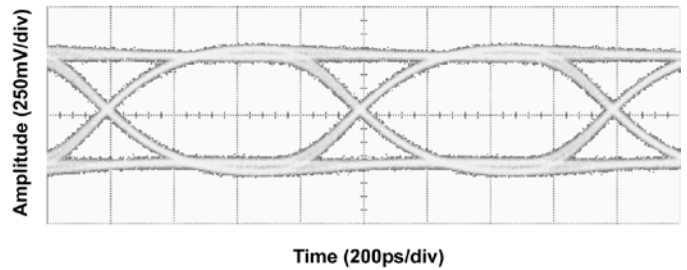
LOS & SD Hysteresis



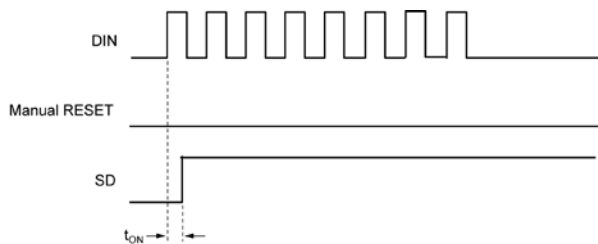
PRBS-23 500mVpp Input @ 1.25Gbps



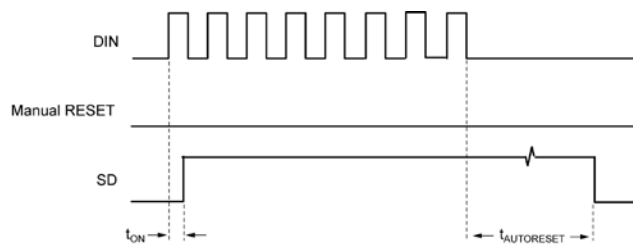
PRBS-23 7.5mVpp Input @ 1.25Gbps



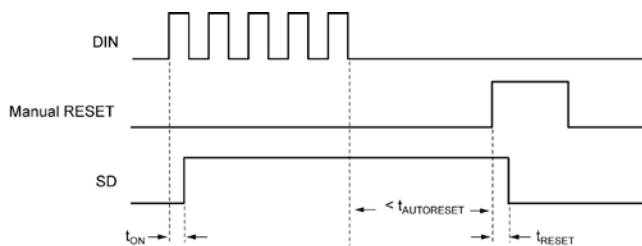
Timing Diagrams



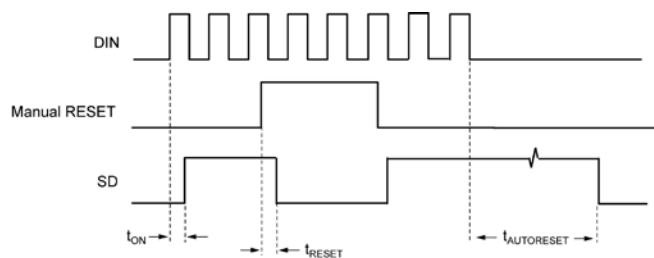
a) No manual RESET & /AutoReset tied HIGH



b) No manual RESET & /AutoReset tied LOW



c) Manual RESET pulse & /AutoReset tied LOW



d) Manual RESET Pulse & /AutoReset tied LOW

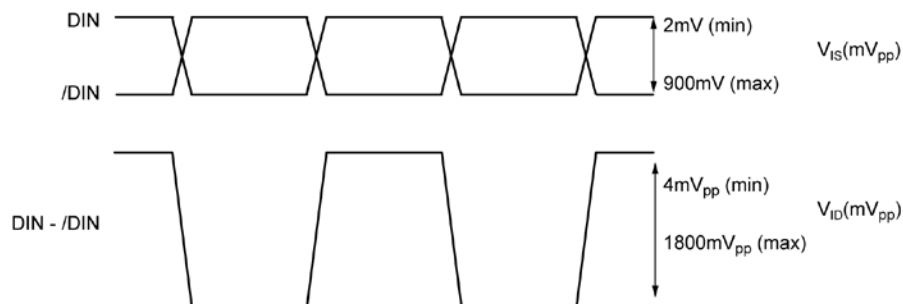


Figure 1. VIS and VID Definition

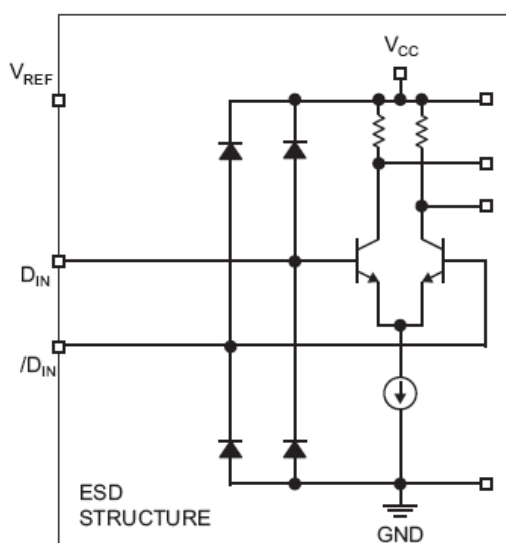


Figure 2. Input Structure

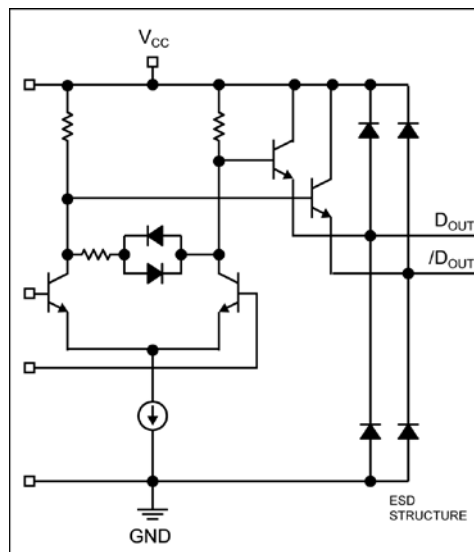


Figure 3. Output Structure

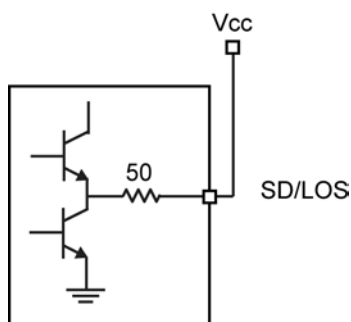


Figure 4. SD Output Structure

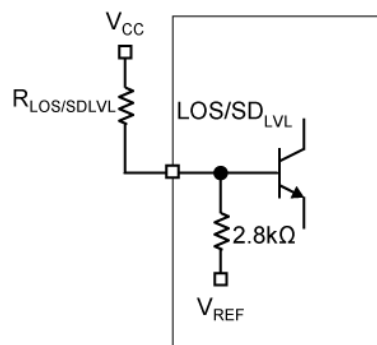
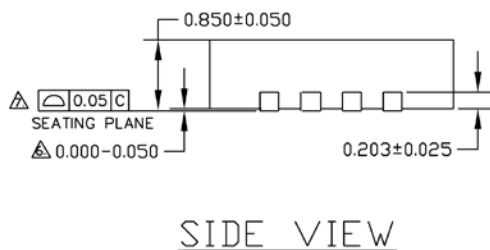
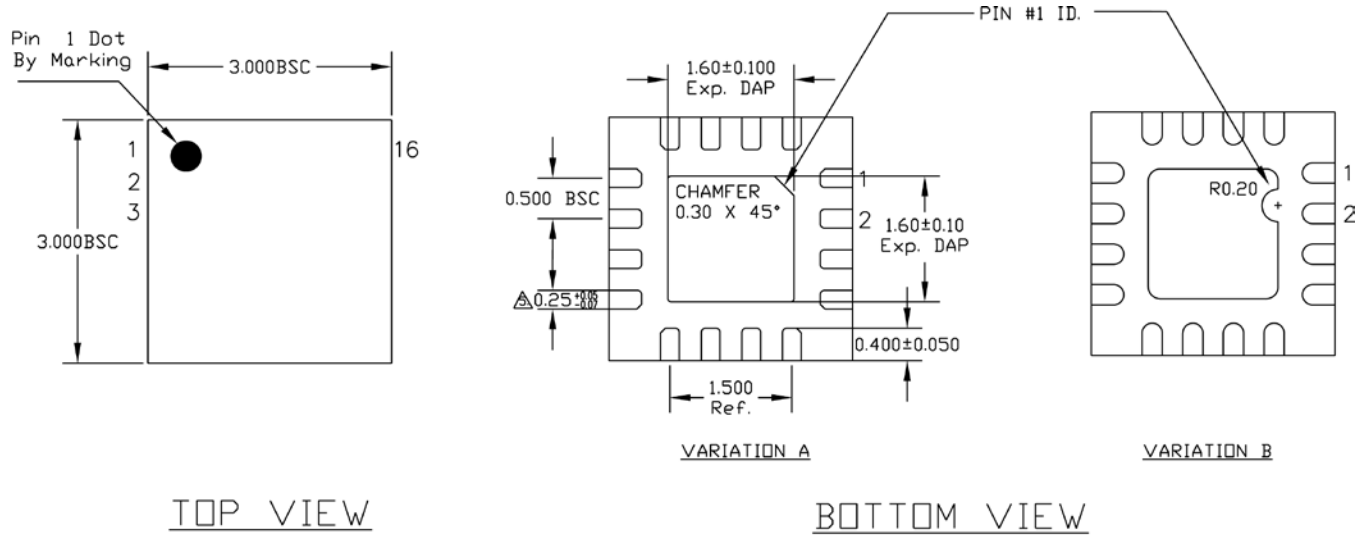


Figure 5. LOS/SDLVL Setting Circuit

Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY88903AL	3.3V, Burst Mode 1.25Gbps PECL High-Sensitivity Limiting Post Amplifier with TTL Loss-of-Signal	http://www.micrel.com/product-info/sy88903al.shtml
SY88149CL	3.3V, 1.25Gbps PECL Limiting Post Amplifier w/High Gain TTL Signal Detect	http://www.micrel.com/product-info/sy88149cl.shtml
Application Notes	Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers	http://www.micrel.com/product-info/app_hints+notes.shtml

Package Information



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

16-Pin QFN

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